REMARKS

Initially, Applicants wish to thank the Examiner for courtesy extended to Applicants' attorney representative in a phone conversation of May 8, 2006 and subsequent e-mail correspondence of May 8 and May 9. During the conversation and in the correspondence, various potential amendments of the independent claims were discussed. No agreement was reached on the claim amendments.

Claims 1-10 are pending in the application. Claims 1 and 9 have each been amended to more particularly point out and claim the invention. In particular, claims 1 and 9 have been amended to recite that the claimed method comprises a step of providing a substrate having at least one gate stack having first and second sidewalls. Support for this amendment is found at least in the original specification in paragraph [0025] and in original Fig. 2. Claims 1 and 9 have been further amended to recite a step of forming first and second separate, unconnected sidewall spacers, the first sidewall spacer extending along at least a portion of the first sidewall and the second spacer extending along at least a portion of the second sidewall. Support for this amendment is found at least in the original specification in paragraph [0026] and in original Fig. 6. No new matter has been added by the foregoing amendments.

Claim Rejection – 35 U.S.C. § 102 – claims 1-10

The Examiner has rejected claims 1-10 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2005/0170104 (Jung *et al.*, hereinafter "Jung"). Regarding claims 1 and 9, the Examiner asserts that Jung discloses in Figs. 1B and related text the method as claimed. In particular, the Examiner points to: substrate 102 having at least one gate stack 110; deposition of a silicon nitride layer 118 by means of a dual-frequency plasma enhanced CVD process comprising a temperature in the range of 375°C to 550°C; formation of a spacer on the at least one gate stack 110 from silicon nitride layer 118; and forming a PFET device 100 comprising the at least one gate stack 110 having spacer 118. Applicants respectfully traverse the rejection of claims 1-10.

Jung discloses a single-layer silicon nitride layer 118 deposited on a substrate 102. The silicon nitride layer 118 is deposited using a plasma-enhanced chemical vapor deposition process

over a polysilicon layer 110. By controlling parameters associated with the deposition process, Jung teaches it is possible to control a stress in the silicon nitride layer.

Independent claim 1 is directed to a method of forming a PFET device, and, as amended, recites, *inter alia*:

> ...
> providing a substrate having at least one gate stack having first and second sidewalls;
> depositing a silicon nitride layer by means of a dual-frequency plasma enhanced CVD process, the CVD process comprising a temperature in the range 400° C to 550° C;
> forming from said silicon nitride layer **first and second separate, unconnected sidewall spacers**, the first sidewall spacer extending along at least a portion of the first sidewall and the second spacer extending along at least a portion of the second sidewall; .... (Emphasis added.)

Independent claim 9 is directed to a method of forming a PFET device, and, as amended, recites, *inter alia*:

> ...
> providing a substrate having at least one gate stack having first and second sidewalls;
> depositing a silicon nitride layer by means of a dual-frequency plasma enhanced CVD process, the CVD process comprising a temperature in the range 400° C to 550° C, a pressure in the range 2 Torr to 5 Torr, a low frequency power in the range 0 W to 50 W, a high frequency power in the range 90 W to 110 W, and precursor gases of silane, ammonia and nitrogen at flow rates in the ratio about 240:3200:4000 sccm;
> forming from said silicon nitride layer **first and second separate, unconnected sidewall spacers**, the first sidewall spacer extending along at least a portion of the first sidewall and the second spacer extending along at least a portion of the second sidewall;.... (Emphasis added.)

Jung fails to disclose at least the feature recited in claims 1 and 9, as amended, of forming **first and second separate, unconnected sidewall spacers** on first and second sidewalls of a gate stack. The silicon nitride layer 118 of Jung is disclosed to be **continuous**, with the sidewall portions of the silicon nitride film 118 connected by a top portion, thus forming **a single, unitary**

structure extending over both the sidewalls and top of polysilicon layer 110, rather than disclosing two **separate, unconnected** sidewall spacers.

Applicants further note that Jung teaches away from the claimed separate, unconnected sidewall spacers. The invention of Jung is directed to the concept of controlling the stress state in the silicon nitride film 118 to control a strain state in the semiconductor device. By providing a single, unitary structure, the stress in the silicon nitride film 118 can be maintained across polysilicon layer 110. Providing two separate, unconnected sidewall spacers obviously would not allow forces (and thus stress and strain) to be communicated across the polysilicon layer 110. The artisan would thus recognize no motivation to modify the single, unitary silicon nitride film 118 of Jung to provide two, separate, unconnected sidewall spacers as recited in claims 1 and 9.

Jung fails to disclose each and every feature of claim 1, as amended (as well as claims 2-8 depending from claim 1) and each and every feature of claim 9, as amended (as well as claim 10 depending from claim 9). Accordingly, it is respectfully requested that the rejection of claims 1-10 under 35 U.S.C. § 102(e) be withdrawn.

CONCLUSION

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application, including claims 1-10, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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(Date)

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